IN THE CLAIMS

Please cancel Claims 1-10 without prejudice, and add Claims 11 through 32 as follows:

11. (New) A method of monitoring the internal operation of a processor, said processor comprising one or more internal buses, said internal buses not accessible from said interfaces, said method comprising:

providing a trigger condition input via at least one of said external interfaces;

providing a monitor input from at least one of said buses;

providing bus data from at least one of said buses;

generating a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event associated with said monitor input;

storing said bus data in response to said trigger output; and

reading at least a portion of said data to a bus trace output.

12. (New) The method of Claim 11, wherein said act of generating comprises generating said trigger output when a predetermined state occurs on a plurality of said buses.

13. (New) The method of Claim 11, wherein said monitor input comprises an address, and said act of generating comprises generating said trigger output when said address falls within a predetermined range of addresses specified by said trigger condition.

14. (New) The method of Claim 11, wherein said act of generating said trigger output comprises:

detecting a first pattern of data within said monitor input;

comparing said first pattern to a second pattern specified within said trigger condition input; and

when at least a portion of said first and second patterns match, generating said trigger output.

15. (New) The method of Claim 11, wherein the bus trace output comprises a test access port which complies with the data transfer protocol as specified in IEEE Standard 1149.1.

16. (New) The method of Claim 11, wherein said processor further comprises a plurality of external interfaces, and said acts of providing a trigger condition input and reading to a bus trace output utilize at least one of said external interfaces.

17. (New) A method of monitoring processor bus states occurring on at least one of a plurality of internal processor buses, the method comprising:

providing a trigger condition;

comparing said trigger condition with an event occurring on at least one of said buses;

continuously storing in a substantially circular fashion a data trace occurring on at least one of said buses in response to a match obtained during said act of comparing; and

providing said trace from said monitor to another device.

18. (New) A method of operating a bus monitor co-located with a processor on a chip, circuit module or circuit board, said chip, module or board having a plurality of external contacts, said processor having a plurality of buses at least some of which are accessible from said contacts, said method comprising:

providing a trigger condition input;

generating a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event obtained from at least one of said buses; and

continuously writing data from at least one of said buses until the occurrence of said trigger output;

storing at least a portion of said data in response to said trigger output; and

providing at least a portion of said data via at least one of said external contacts.

19. (New) The method of Claim 18, wherein said act of providing a trigger condition input comprises providing said trigger condition input via at least one of said plurality of external contacts.

20. (New) A method of monitoring the internal operation of a processor comprising at least one external interface and at least one internal bus, said internal bus not directly accessible from said at least one interface, said method comprising:

providing a trigger condition via said at least one external interface;

providing a first signal from said at least one bus;

providing data from said at least one bus;

generating a second signal when information associated with said trigger condition satisfies a predetermined relationship to an event associated with said first signal;

storing said data based at least in part on said second signal; and

transferring at least a portion of said data to an output.

21. (New) The method of Claim 20, wherein said act of providing a trigger condition comprises providing said trigger condition via said at least one external interface.

22. (New) A method of monitoring the internal operation of a processor, said processor comprising one or more internal buses, said internal buses not accessible from external interfaces, said method comprising the steps of:

a step for providing a triggering condition;

a step for generating a monitor signal from at least one of said buses;

a step for transferring bus data from at least one of said buses;

a step for generating a trigger output when said trigger condition compares to a trigger event associated with said monitor signal;

a step for storing said bus data based at least in part on said trigger output; and

a step for providing at least a portion of said data to a bus data output.

23. (New) A method of monitoring the internal operation of a processor, said processor comprising a plurality of external interfaces and one or more internal buses, said internal buses not accessible from said interfaces, said method comprising:

providing a trigger condition input;

providing a monitor input from at least one of said buses;

providing bus data from at least one of said buses;

generating a first trigger output when a trigger condition derived from said trigger condition input compares to a trigger event associated with said monitor input;

incrementing a counter in response to said trigger output in order to count a number of trigger events; and

when said counter reaches a predetermined count, generating a second trigger output to indicate the predetermined number of trigger events have been observed.

24. (New) The method of Claim 23, further comprising:

in response to the second trigger, coupling a set of internal processor state information to at least one of said external interfaces.

25. (New) The method of Claim 24, wherein said at least one external interface to which the internal processor state information is coupled comprises a test access port.

26. (New) The method of Claim 25, wherein said test access port implements a set of pins and data transfer protocols that comply with IEEE Standard 1149.1.

27. (New) The method of Claim 24, further comprising:

continuously storing in a substantially circular fashion a data trace occurring on at least one of said buses;

wherein said information of internal processor state comprises said data trace.

28. (New) The method of Claim 24, further comprising:

continuously generating a set of data trace data occurring on at least one of said buses;

wherein said set of internal processor state information comprises said data trace data.

29. (New) A method of monitoring processor bus states occurring on at least one of a plurality of internal processor buses, the method comprising:

providing a trigger condition;

comparing said trigger condition with an event occurring on at least one of said buses;

generating a data trace occurring on at least one of said buses in response to a match obtained during said act of comparing; and

coupling said trace to a test access port that implements a data transfer protocol that complies with IEEE Standard 1149.1.

30. (New) A method of monitoring the internal operation of a processor, said processor comprising a plurality of external interfaces and one or more internal buses, said internal buses not accessible from said interfaces, said method comprising:

providing a trigger condition input;

providing a monitor input from at least one of said buses;

providing bus data from at least one of said buses;

generating a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event associated with said monitor input;

in response to said trigger output, causing at least one word to be read into an instruction register associated with a test access port.

31. (New) The method of Claim 30, wherein said test access port complies with IEEE Standard 1149.1.

32. (New) The method of Claim 30, wherein the one data word represents volatile state information that is coupled to an external debugging device via said test access port.